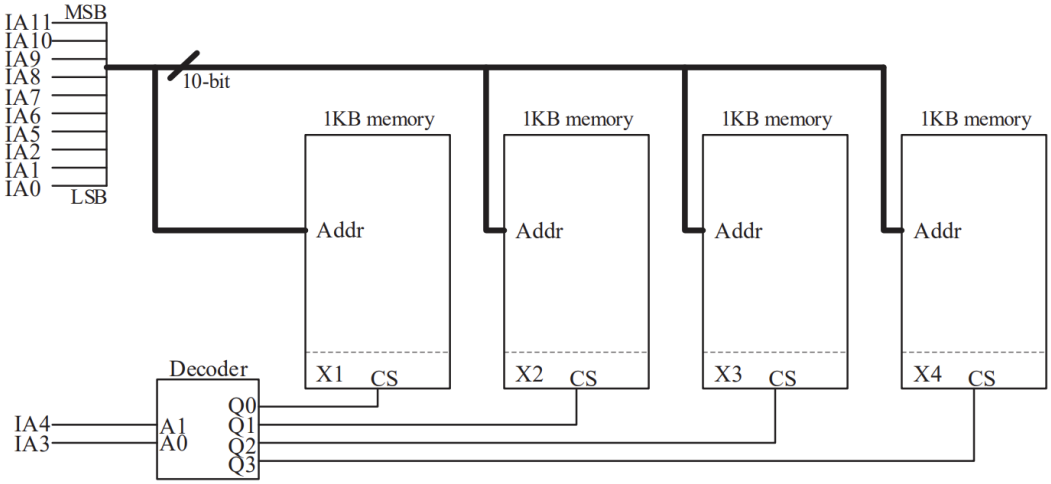
Malaviya National Institute of Technology Jaipur
Department of Computer Science Engineering
Computer Architecture CP-226
Mid-sem Examination, Date: March 1, 2024

Time: 4:15 pm-5:45 pm (1.5 hours) Spring 2024, IV Semester Max marks: 30

Instructions:

1. All questions are compulsory.
2. This paper has two pages, please turn it over.
3. Be precise in your answers.

1. (a) A 4 kilobyte(KB) byte-addressable memory is realized using four 1 KB memory blocks. Two input address lines (IA4 and IA3) are connected to the chip select (CS) port of these memory blocks through a decoder as shown in the figure. The remaining ten input address lines from (IA11-IA0) are connected to the address port of these blocks. The chip select (CS) is active high.



The input memory addresses (IA11-IA0) in decimal, for the starting locations (Addr=0) of each block (indicated as X1, X2, X3, X4 in the figure). What are the values of (X1, X2, X3, X4)? Explain in detail. **(5)**

2. (a) For each of the following cases, state whether SRAMs or DRAMs would be appropriate building blocks for the memory system, and explain why. Assume that there is only one level in the memory hierarchy.
   1. A memory system where performance was the most important goal.
   2. A memory system where cost was the most important goal.
   3. A design where data need to be stored for long periods without any action on the processor's part. **(3)**

   (b) Dynamic RAM has a memory cycle time of 64 nsec. It has to be refreshed 100 times per msec and each refresh takes 100 nsec. What percentage of the memory cycle time is used for refreshing? **(2)**

3. (a) Consider a 2-way set associative cache memory with 4 sets and a total of 8 cache blocks (0-7) and a main memory with 128 blocks (0-127). What memory blocks will be present in the cache after the following sequence of memory block references if LRU policy is used for cache block replacement? Assuming that initially, the cache did not have any memory block from the current job. Also, explain why.

   0 5 3 9 7 0 16 55 **(3)**

   (b) More than one word is put in one cache block to exploit the _____ locality of reference in a program. **(1)**

   (c) Why does increasing the associativity of a cache generally increase its hit rate? **(1)**

4. A memory system has 32-bit virtual addresses, 20-bit physical addresses, and 4 kB pages.

   (a) How big is each page table entry if a single-level page table is used? (Round up to the nearest byte.) **(2)**

   (b) How many page table entries are required for this system? **(2)**

   (c) How much storage is required for the page table (single-level page table)? **(1)**

5. (a) Explain RISC and CISC instruction set architectures in detail with some real-life processor examples. What are their advantages and disadvantages? **(5)**

6. (a) What is the difference between indirect addressing and register indirect addressing? Explain in terms of memory accesses and addressing space. **(5)**

*****Best wishes*****