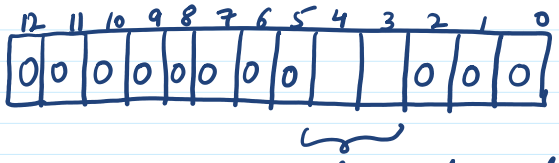
Mid-sem Answer key

03 March 2024 12:58

1.



Active high chip select (CS)

12 bits address

⇒ For starting address, I11 – I5 remains 0.

⇒ Four possible combinations

	I4	I3	I11 - - I0	In decimal
X0	0	0	00000	0
X1	0	1	01000	8
X2	1	0	10000	16
X3	1	1	11000	24

⇒ (X0, X1, X2, X3) ⟶ (0, 8, 16, 24)

2. (a). 1. SRAMs generally have low latencies than DRAMs.

2. DRAMs have lower cost/bit than SRAMs.

3. SRAMs are better than DRAMs since DRAMs have to have their contents refreshed in order to store for long period of time.

(b) Cycle time = 64 nsec

Refresh rate = 100 times / msec

Time of one refresh = 100 nsec

No. of refreshes (10^{-3} sec) = 100

No. of refreshes 1 sec = $\frac{100}{10^{-3}}$

No. of refreshes 64 nsec = $\frac{100}{10^{-3}} \times 64 \times 10^{-9}$

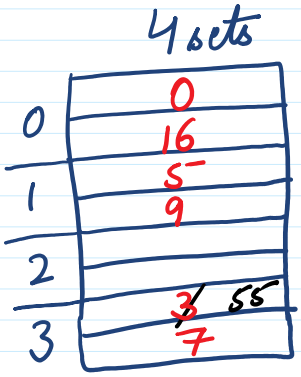
Total time spent in refresh = 100 nsec $\times \frac{100}{10^{-3}} \times 64 \times 10^{-9}$

= .64 nsec

% of memory cycle time used for refreshing = $\frac{0.64 \text{ nsec}}{64 \text{ nsec}} \times 100$

= 1%

3. (a) Given sequence of memory block references 0 5 3 9 7 0 16 55



Miss → 0 % 4 → 0

Miss → 5 % 4 → 1

Miss → 3 % 4 → 3

Miss → 9 % 4 → 1

Miss → 7 % 4 → 3

Hit → 0 → LRU

Miss → 16 % 4 → 0

Miss → 55%4 → 3 (Replacing 3 as LRU replacement policy is used)

⇒ The final sequence is 0, 16, 5, 9, 55, 7

(b) Spatial

(c) Lecture - 14

4. Given, 32-bit virtual address, 20-bit physical address, and 4KB pages.

(a) Page table entry size?

Page size = 4kB

⇒ 12 bits are required for offset.

Physical Page Number

8 bits = 1 byte

Or there are 2 extra bits also needed in general, so 10 bits = 2 bytes

⇒ 1byte / 2byte

both answers are correct.

(b) Number of page table entries?

Virtual address space = 2^{32}

Page size = 4KB = 2^{12}

$\Rightarrow$ No of page table entries = $\frac{2^{32}}{2^{12}} = 2^{20}$

(c) Storage required for the page table?

Each page table entry requires 1/2 bytes.

$\Rightarrow$ Total storage required = 1/2 bytes $\times 2^{20}$

$= 2^{20}/2^{21}$ bytes.

5.- Lecture -6

6. - Lecture -5