Malaviya National Institute of Technology Jaipur
Department of Computer Science Engineering

Computer Architecture CP-226

Mid-sem Quiz, Date: April 23, 2024

Time: 3:15 pm-3:45 pm Spring 2024, VI Semester

Name: _____.

Roll No.: _____.

1. Which of the following is not a pipeline hazard?
   (a). Data Hazard
   (b). Control Hazard
   (c). Address Hazard
   (d). Structural Hazard

2. Consider a pipeline processor operating at 2 GHz with 5 stages. Each stage except execute(EX) stage takes one cycle for ADD and SUB, three cycles for MUL, two cycles for DIV instruction. Consider the following instructions:
   I_1 : ADD R_1, R_2, R_3;
   I_2 : SUB R_3, R_2, R_1;
   I_3 : MUL R_4, R_1, R_2;
   I_4 : DIV R_3, R_4, R_3;
   The above code has _____ number of data dependencies and the execution time using forwarding techniques is _____.
   (a). 5, 5.0ns
   (b). 3, 5.5ns
   (c). 3, 4.2ns
   (d). 2, 3.0ns

3. In a processor-based system, a DMA facility is required to increase the speed of the data transfer between the
   (a). Processor and the memory.
   (b). Processor and I/O devices.
   (c). Memory and I/O devices.
   (d). Memory and register.

4. A hard disk with a transfer rate of 10 Mbytes/ second is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation?
   (a). 5.0%
   (b). 1.0%
   (c). 0.5%
   (d). 0.1%

5. Given below are three statements related to interrupt handling mechanism
   A. Interrupt handler routine is not stored at a fixed address in the memory.
   B. CPU hardware has a dedicated wire called interrupt request line used for handling interrupts.
   C. Interrupt vector contains the memory addresses for specialized interrupt handlers.

   (a). Only A is TRUE.
   (b). Both B and C are TRUE.
   (c). Both A and C are TRUE.
   (d). Both A and B are TRUE.

*****Best wishes*****