Lecture-9 (Memory Systems)

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→ Memory is used to store instructions and data.

(0's and 1's)

→ Byte addressable :-

A memory is said to be byte addressable if every byte of data has a unique address.

1 byte = 8 bits has a unique address

→ Word addressable :-

Let 1 word = 4 bytes
= 32 bits

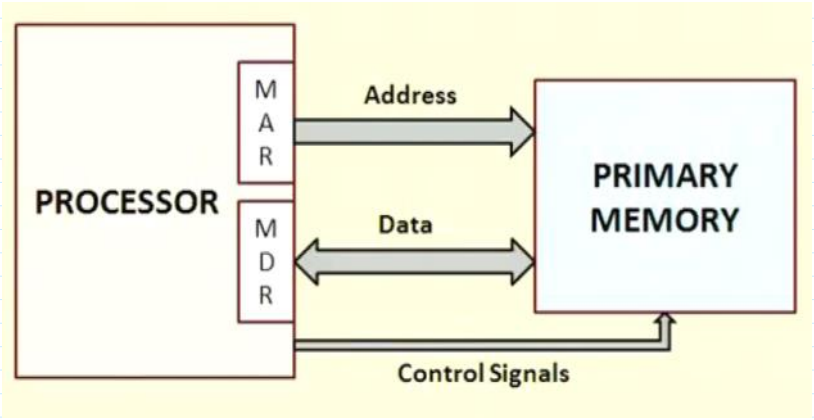
Then memory address will be incremented by 4.

0, 4, 8, and so on.

Let 1 word = 8 bytes
= 64 bits

0, 8, 16, and so on.

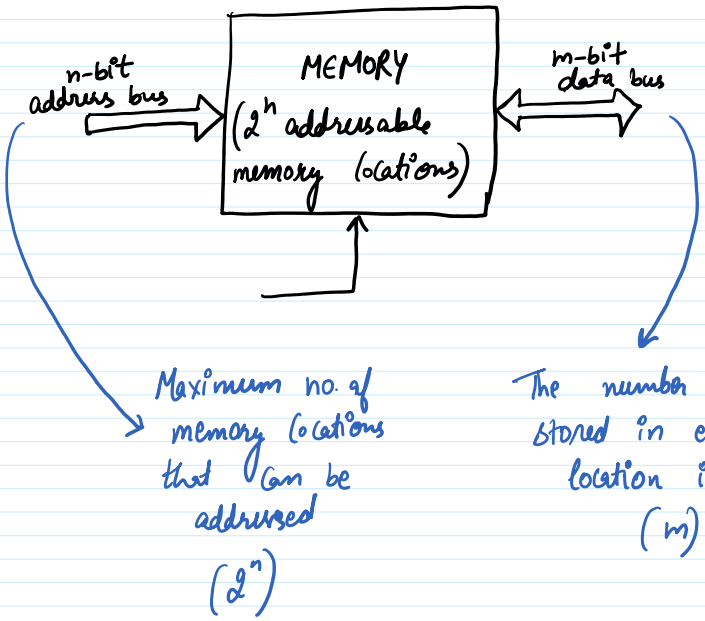
Processor and Memory :-



① Memory Address Register (MAR)
Address of data/instruction to be read or written.

② Memory Data Register (MDR)
Data to be read/written.
Bidirectional.

③ Control Signals, READ, WRITE etc.



Total memory size = $2^n \times m$

(a) Volatile v/s Non-volatile

Volatile :- The stored data is lost when power is switched off.
CMOS static & dynamic Memories.

Non-volatile :- Data is retained when power is switched off.
Read Only Memories :-
CD ROM, DVD, etc...

(b) Random / Sequential / Direct Access Memory :-

Random Access :-
When read/write time is independent of memory location being accessed.
→ RAM and ROM

Sequential Access :-
when stored data can only be accessed in a particular order.
→ Magnetic tape

Direct Access :-
(Semi-random access)
when part of the access is random and part is sequential.
→ Magnetic Disk

(c) Read-only v/s Random-access :-

Read-only Memory (ROM)

→ data programmed during manufacturing or in the laboratory.
(permanent / semi-permanent)
→ ROM, PROM, EPROM, etc.

Random-access Memory (RAM)
→ used in main memory and cache memory.
→ Static RAM & Dynamic RAM

Terminologies :-

Memory Access Time :-
Time between initiation of a operation and completion of that operation.

Latency :-
Initial delay from the initiation of an operation to the time the first data available.

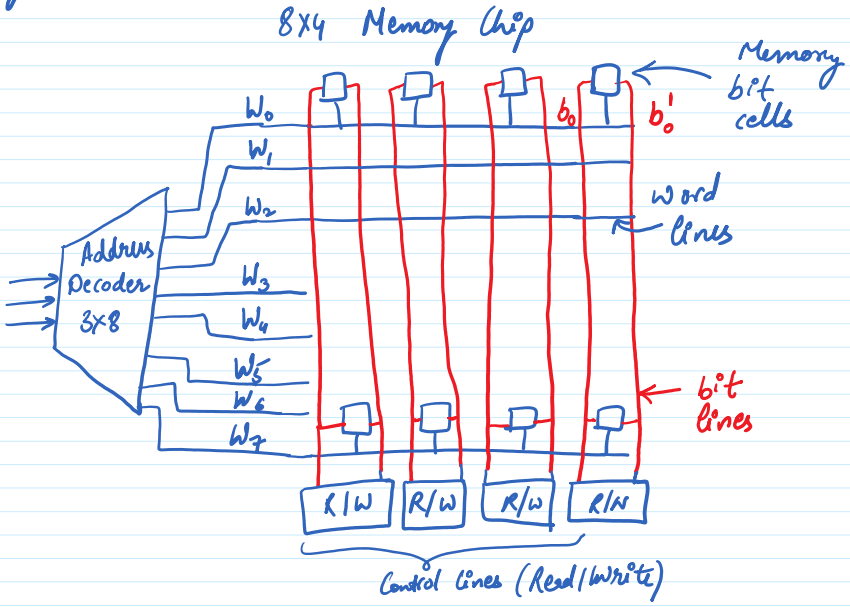
Bandwidth :-
Maximum speed of data transfer in bytes per second.

Memory Goals :-

① Make memory system work faster.
② Increase the data transfer rate between CPU and memory.
③ Increase the storage need.

Solutions :-
① Cache Memory :- ↑ effective speed.
② Virtual Memory :- ↑ effective size.

Memory Chip Organization :-

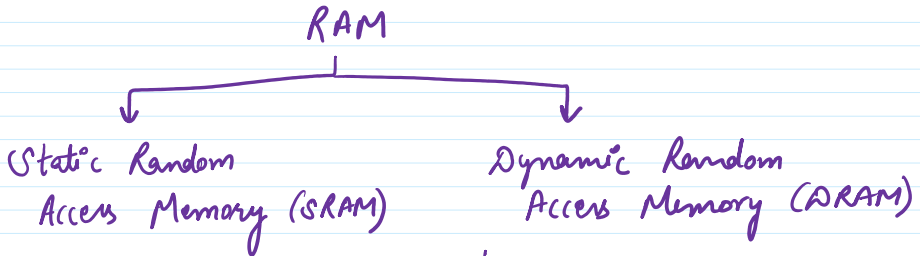


→ 32-bit Memory

→ 3×8 decoder is required to access any word out of 8 words. (8 rows)

→ Two bit lines
bit b and it's complement b'.
for reading and writing

RAM Organization



→ Asynchronous DRAM

→ Synchronous DRAM

* Present day main memory systems are build using

Difference in terms of :-

Speed → how fast

Density → How many bits can be packed.

Volatility → If power supply is off.

Quiz :-

Register Indirect v/s Indirect Addressing.
(RI) (IA)

(a)
RI : Less Address Space
More Memory Access
IA : Large Address Space
Less Memory Access

(b)
RI : More Address Space
Less Memory Access
IA : Large Address Space
More Memory Access

(c)
RI : Large Address Space
Less Memory Access
IA : Less Address Space
More Memory Access

(d)
RI : Large Address Space
Less Memory Access
IA : Less Address Space
Less Memory Access