Lecture-30: Pipelining Hazards

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Hazards :- Situations that prevent a pipeline from operating at its maximum possible clock speed.

→ Prevents some instructions from executing during its designated clock cycle.

Types of hazards

① Structural Hazard
→ resource conflicts

② Data Hazard
→ data dependencies between instⁿ.

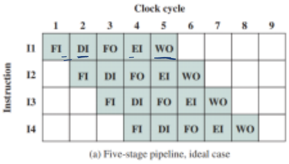
③ Control Hazard
→ branch and other instructions.

Structural Hazard :-

When two or more instructions that are already in the pipeline need the same resource.

Example :-

Ideal Pipelining :→

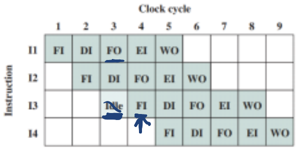


Clock cycle

Instruction	1	2	3	4	5	6	7	8	9
I1	FI	DI	FO	EI	WO				
I2		FI	DI	FO	EI	WO			
I3			FI	DI	FO	EI	WO		
I4				FI	DI	FO	EI	WO	

(a) Five-stage pipeline, ideal case

Memory has a single port
I1 is in memory



Clock cycle

Instruction	1	2	3	4	5	6	7	8	9
I1	FI	DI	FO	EI	WO				
I2		FI	DI	FO	EI	WO			
I3			Idle	FI	DI	FO	EI	WO	
I4					FI	DI	FO	EI	WO

(b) I1 source operand in memory

Can insert "stall cycles" in the pipeline.

$$\text{Speed-up, } S_k = \frac{T_{1,n}}{T_{k,n}} = \frac{T_{NP}}{T_P} = \frac{CPI_{NP} \times C_{NP}}{CPI_P \times C_P} = \frac{C_{NP}}{C_P} \times \frac{CPI_{NP}}{CPI_P}$$

CPI → Cycles per instⁿ

C → Clock Cycle Time

$$\boxed{\text{Speed-up, } S_k = \frac{C_{NP}}{C_P} \times \frac{CPI_{NP}}{CPI_P}} \text{ — } (i)$$

Through pipelining we are reducing CPI or C.

Ideal CPI of an Instⁿ pipeline can be written as,

$$CPI_{NP} = \text{Ideal CPI} \times \text{Pipeline Depth}$$

$$\text{Ideal CPI} = \frac{CPI_{NP}}{\text{Pipeline Depth}}$$

$$\text{Speed Up} = \frac{C_{NP}}{C_P} \times \frac{\text{Ideal CPI} \times \text{Pipeline Depth}}{CPI_P}$$

$$CPI_P = \text{Ideal CPI} + (\text{Pipeline Stall Cycles per Inst}^n)$$

$$\text{Speed Up} = \frac{C_{NP}}{C_P} \times \frac{\text{Ideal CPI} \times \text{Pipeline Depth}}{\text{Ideal CPI} + \text{average pipeline stall cycles / inst}^n}$$

Let $C_{NP} = C_P$

i.e. ignoring the increase in clock cycle time.

$$\boxed{\text{Speed Up} = \frac{\text{Ideal CPI} \times \text{Pipeline Depth}}{\text{Ideal CPI} + \text{Pipeline stall cycles / instruction}}}$$

Example:-

Q:- The ideal CPI of a pipeline is 1.3. Consider there is a structural hazard in which data references constitute 35% of the instructions.

How much faster is the ideal machine without the memory structural hazard, vs machine with the hazard?

$$\boxed{\text{Speed Up} = \frac{\text{Ideal CPI} \times \text{Pipeline Depth}}{\text{Ideal CPI} + \text{Pipeline stall cycles / instruction}}}$$

$$\text{Speed Up}_{ideal} = \frac{1.3 \times \text{Pipeline Depth}}{1.3 + 0}$$

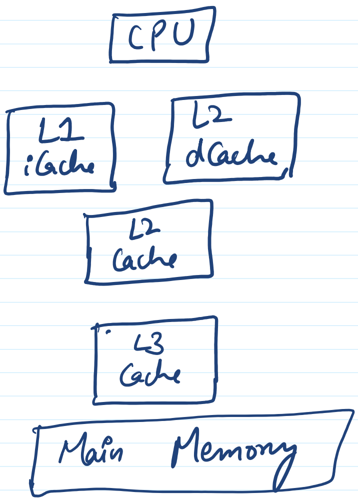
$$\text{Speed Up}_{real} = \frac{1.3 \times \text{Pipeline Depth}}{1.3 + 0.35 \times 1}$$

$$\frac{\text{Speed Up}_{ideal}}{\;} = \frac{1.65}{\;} = 1.27$$

Speed Up real 1.3

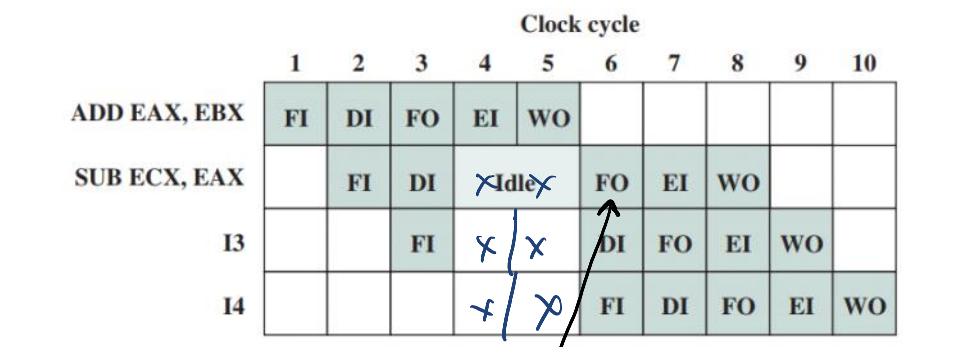
Memory Structural Hazard is quite frequent.

⇒ Makes use of saperate instruction and data caches in the first level



Data Hazards :-

Occurs due to data dependencies between instructions that are various stages of execution in the pipeline.



	Clock cycle									
	1	2	3	4	5	6	7	8	9	10
ADD EAX, EBX	FI	DI	FO	EI	WO					
SUB ECX, EAX		FI	DI	x Idle x		FO	EI	WO		
I3			FI	x	x	DI	FO	EI	WO	
I4				x	x	FI	DI	FO	EI	WO

Figure 14.16 Example of Data Hazard

SUB inst^n can fetch wrong value of EAX without "Stall cycle".

naive way

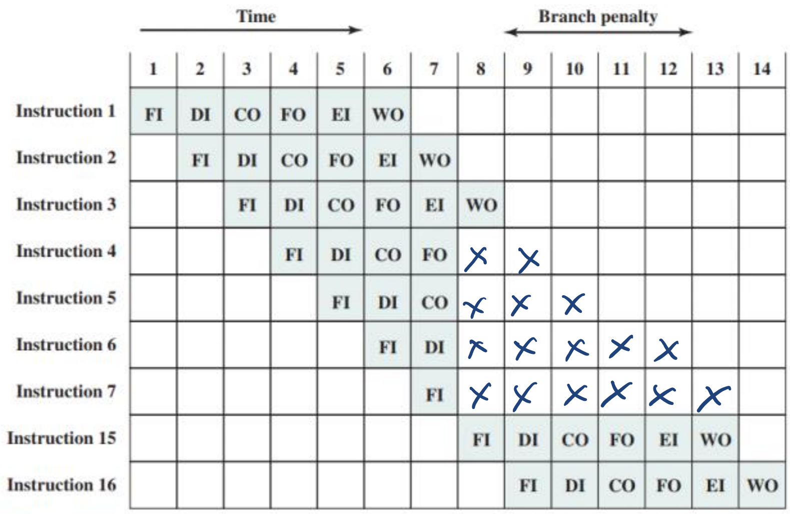
How to reduce the number of stall cycles?

- Data Forwarding/ Bypassing
- Concurrent Register Access

Control Hazard :-

Arises because of branch instructions being executed in a pipeline.

→ Can cause greater performance loss than data hazards.



Time
Branch penalty

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Instruction 1	FI	DI	CO	FO	EI	WO								
Instruction 2		FI	DI	CO	FO	EI	WO							
Instruction 3			FI	DI	CO	FO	EI	WO						
Instruction 4				FI	DI	CO	FO	X	X					
Instruction 5					FI	DI	CO	X	X	X				
Instruction 6						FI	DI	X	X	X	X	X		
Instruction 7							FI	X	X	X	X	X	X	
Instruction 15								FI	DI	CO	FO	EI	WO	
Instruction 16									FI	DI	CO	FO	EI	WO

Figure 14.11 The Effect of a Conditional Branch on Instruction Pipeline Operation

How to reduce the branch panelty?