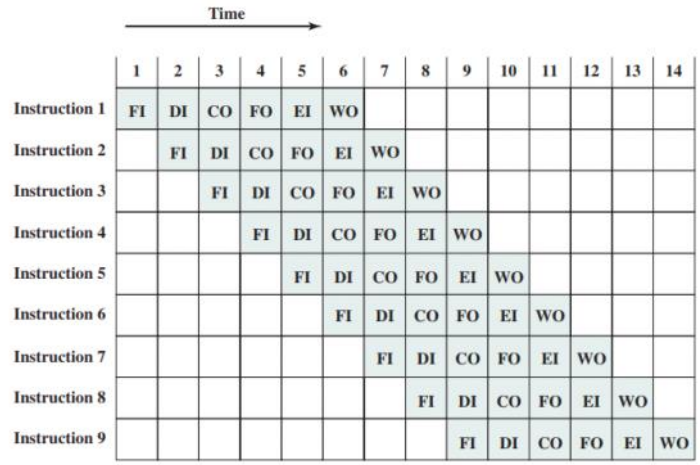
Speed up and Efficiency :-

Let τ be the cycle time of an instruction pipeline.



	Time →													
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Instruction 1	FI	DI	CO	FO	EI	WO								
Instruction 2		FI	DI	CO	FO	EI	WO							
Instruction 3			FI	DI	CO	FO	EI	WO						
Instruction 4				FI	DI	CO	FO	EI	WO					
Instruction 5					FI	DI	CO	FO	EI	WO				
Instruction 6						FI	DI	CO	FO	EI	WO			
Instruction 7							FI	DI	CO	FO	EI	WO		
Instruction 8								FI	DI	CO	FO	EI	WO	
Instruction 9									FI	DI	CO	FO	EI	WO

Figure 14.10 Timing Diagram for Instruction Pipeline Operation

$$\tau = \max_i [\tau_i]$$
$$= \tau_m \qquad 1 \le i \le k$$

$\tau_i \rightarrow$ time in the i^{th} stage of pipeline

$\tau_m \rightarrow$ maximum stage delay.

$k \rightarrow$ number of stages.

Let 'n' be the number of inst^n processed.

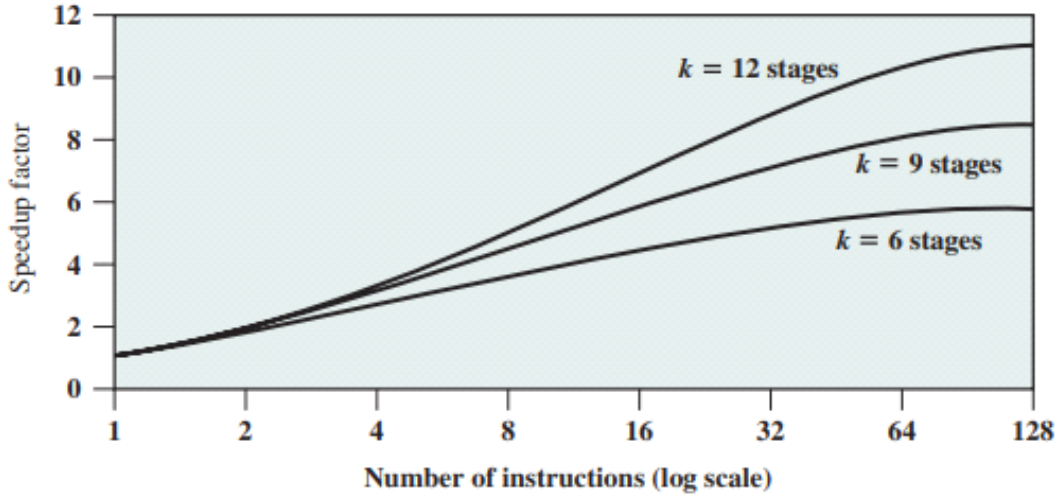
$T_{k,n} \rightarrow$ time required for a pipeline with k stages to execute n instructions.

$$T_{k,n} = [k + (n-1)]\tau$$

In the example, $(6+(9-1))\tau$

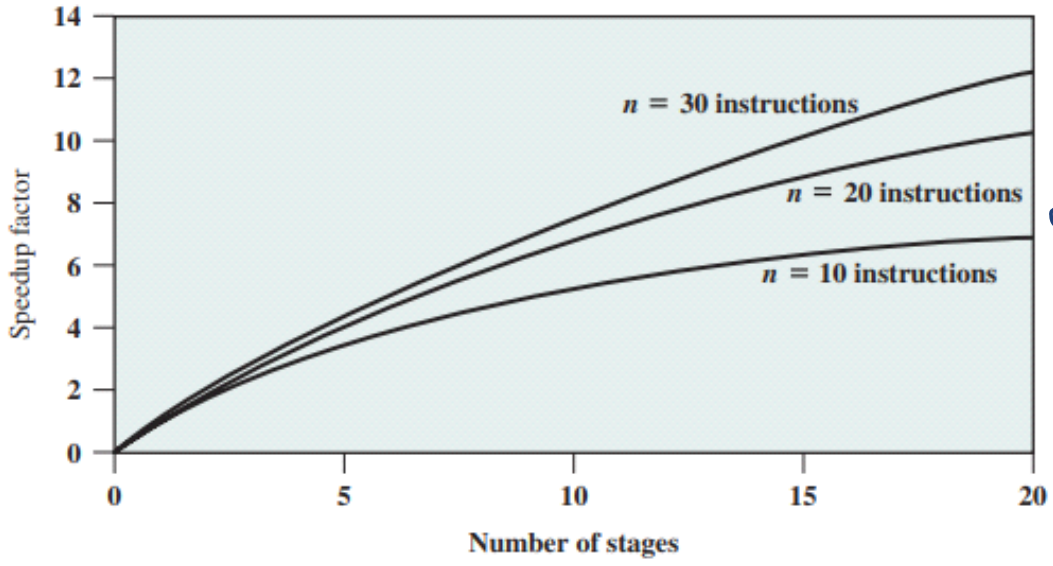
No pipeline $\Rightarrow k=1$

Speed-up, $S_k = \frac{T_{1,n}}{T_{k,n}} = \frac{nk\tau}{(k+(n-1))\tau} = \frac{nk}{k+(n-1)}$



$S_k \propto k$

(a)



$S_k \propto n$

(b)

Figure 14.14 Speedup Factors with Instruction Pipelining