Lecture-24 : Direct Memory Access

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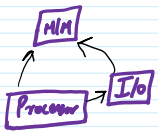
Programmed I/O requires active intervention of processor.



Drawbacks :-

① I/O transfer is limited by the speed with which the processor can test and service a device.

② Managing I/O transfers is an overhead for the processor.

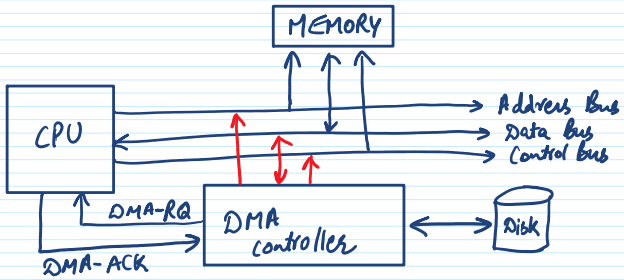
③ Not suitable for large data transfers, eg. files in GBs.

Direct Memory Access :- (DMA)

I/O ↔ Memory with least invention in the processor.

Programmed I/O < Interrupt-driven I/O < Direct Memory Access < I/O Processors

DMA controller is a hardwired controller which enables direct data transfer between I/O device and memory.



In this scenario,

⇒ by default processor is bus master.

⇒ If the DMA controller needs the bus control, it initiates a signal (DMA-RQ)

⇒ After getting DMA-ACK signals processor releases the control and DMAC becomes the bus master.

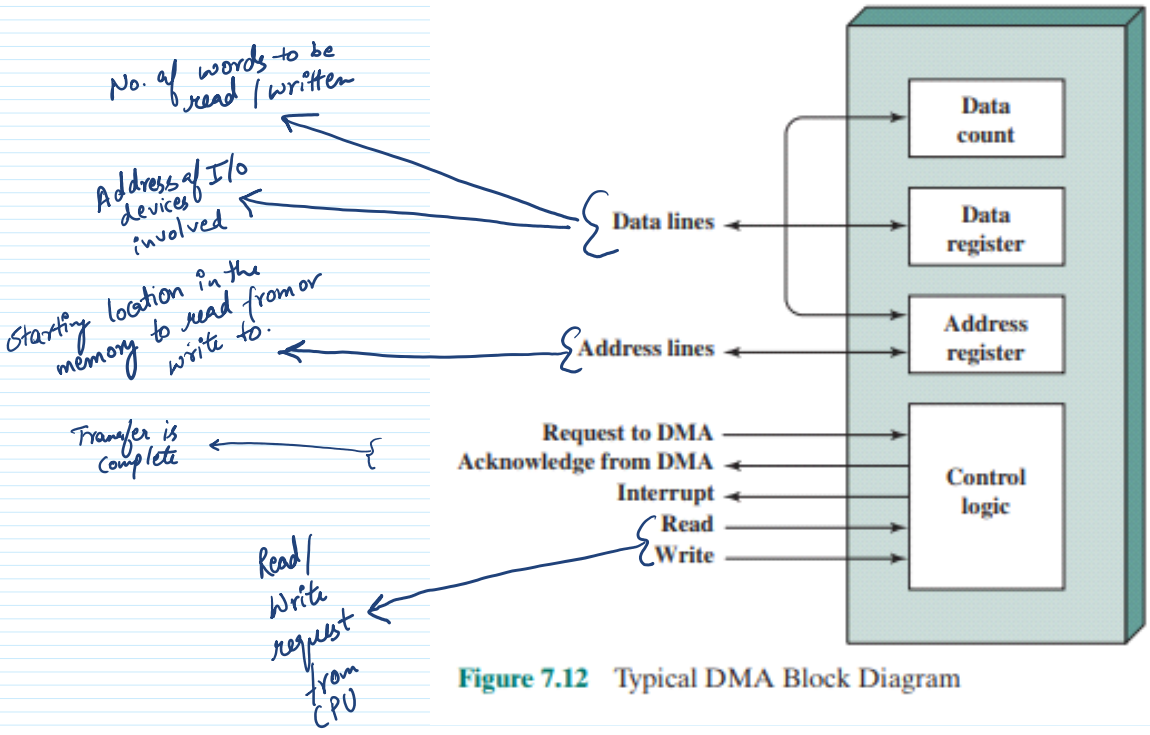


Figure 7.12 Typical DMA Block Diagram

When processor wants to read/write a block of data, it issues following information to the DMA module :-

① Read / Write ?
② Address of I/O device involved.
③ Starting location in the memory.
④ No. of words to be read/written.

Then the processor continues with other work or keep idle.
DMAC do its work of transferring data.
After completion sends the interrupt signal.
" Thus processor is involved only in beginning and end."

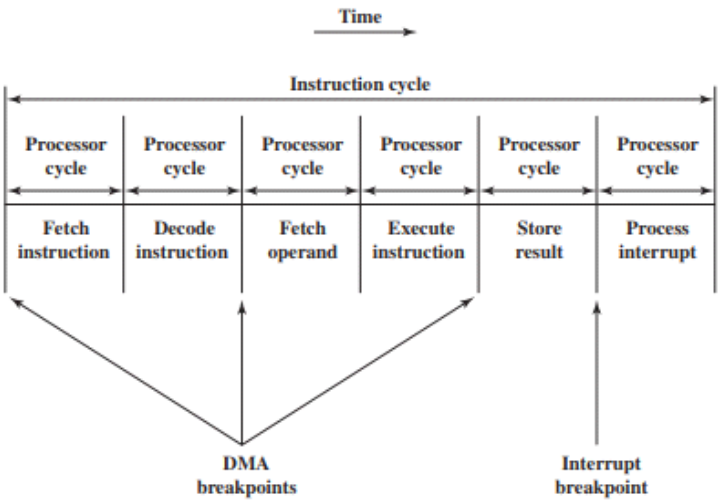


Figure 7.13 DMA and Interrupt Breakpoints during an Instruction Cycle

The processor is suspended just before it needs to use the bus.

The processor will not be interrupted, it will only pause.

DMA Configurations :-

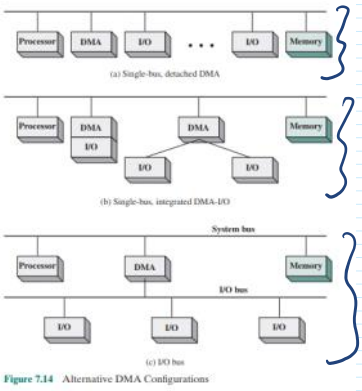


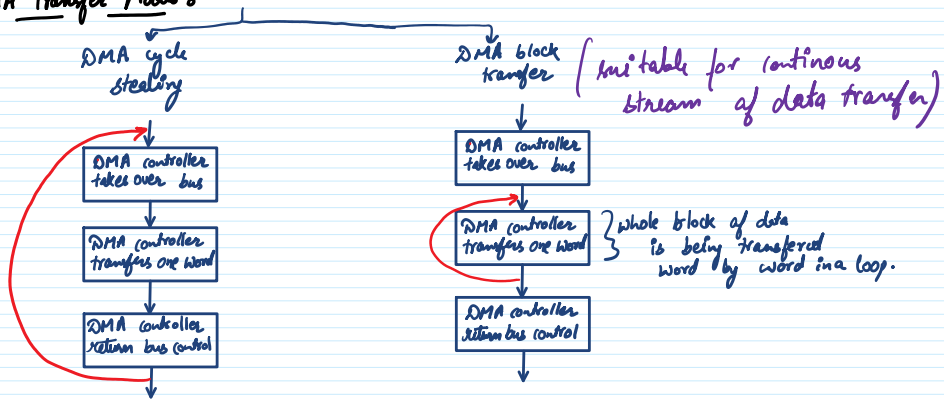
Figure 7.14 Alternative DMA Configurations

All modules shares the same system bus

path between DMA and I/O modules

Seperate I/o bus connecting I/O modules to DMA module.

DMA Transfer Modes :-



① DMA controller requests CPU for a few cycles.

② Preferably when CPU is not using memory.

③ DMA controller has stealed the cycle without CPU knowing it.

① DMA controller transfers the whole block of data without interruption.

② Results in maximum possible data transfer rate.

③ CPU will remain idle during this time.

Q:- A DMA module is transferring one 8-bit character in one CPU cycle from a device to memory through cycle stealing at regular intervals. Consider a 2MHz processor. If 0.5% processor cycles are used for DMA, the data transfer rate of the device is ____ bits per second.

1 sec —— 2×10^6 cycles

For DMA, in 1 sec —— 0.5% of 2×10^6

$= 0.5 \times 2 \times 10^6$

$= 10,000$ cycles

In DMA, 8-bits for 1 cycle $\Rightarrow$ $8 \times 10,000$ bits/sec

Q:- A DMA module is transferring bytes to main memory from an external device at 76800 bps. The CPU can fetch instructions at a rate of 2 million instructions

per second. Assume instruction size is 32 bits. How much will the processor be slowed down due to DMA activity?

In 1 sec — CPU → 2M × 32 bits

DMA → 76800 bits

$$\text{Slow down} = \frac{76800}{64M} \times 100\ \%$$