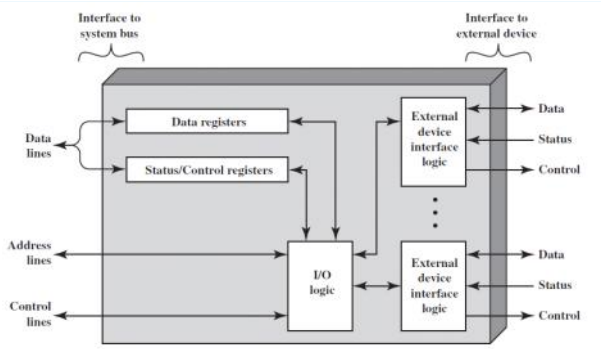
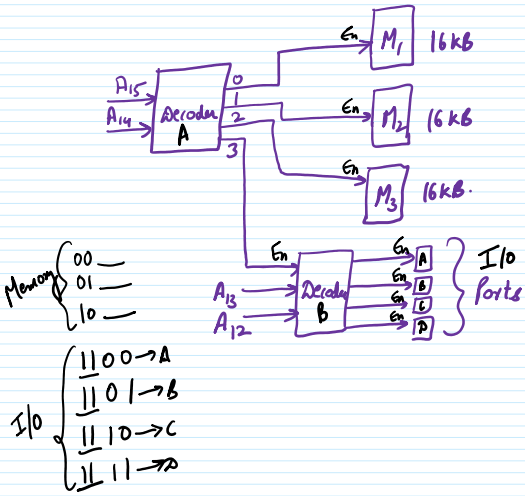


Figure 7.3 Block Diagram of an I/O Module

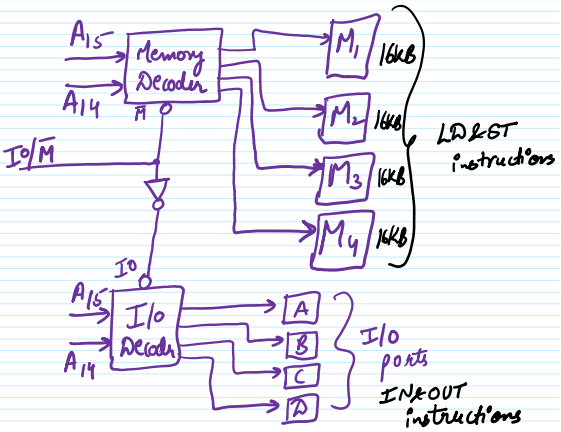
Types of Device Interfaces :-

Ways of connecting the I/O devices to the address and data buses.

Memory-Mapped Device Interface



I/O Mapped Device Interface



Memory-Mapped Device Interface	I/O Mapped Device Interface
① Same address decoder selects memory and I/O ports.	① Separate instructions for I/O data transfer (IN/OUT).
② Some of the memory address space is occupied by I/O devices.	② A processor signal identifies whether a generated address refers to a memory location or an I/O device.
③ All data transfer instructions to/from memory can be used to transfer data to/from I/O devices.	③ Separate address decoders for selecting memory and I/O ports.
④ The processor need not have separate instructions for I/O, no I/O/$\overline{M}$ address signal.	④ The complete address space can be utilized.

Modes of Data Transfer :-

How the actual data transfer takes place between the I/O devices and the processor.

Table 7.1 I/O Techniques

	No Interrupts	Use of Interrupts
I/O-to-memory transfer through processor	Programmed I/O	Interrupt-driven I/O
Direct I/O-to-memory transfer		Direct memory access (DMA)

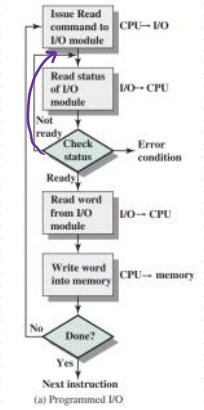
M/M

Processor

I/O

① Programmed I/O :- Data is exchanged between processor and I/O module.

Programmed I/O



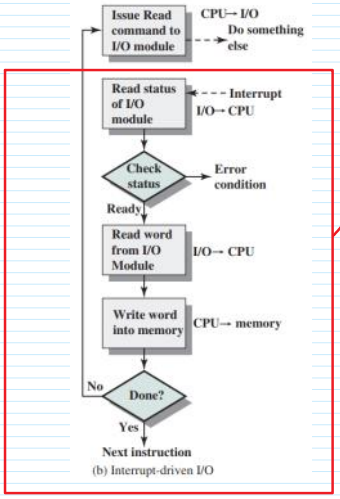
→ ① Synchronous :→ → I/O device transfers data at a fixed rate and is also known to the CPU.
→ CPU lies idle during time delay
→ Not all devices have strictly synchronous transfer speed.

→ ② Asynchronous :→ → CPU does not know when the I/O module will be ready to transfer the next word.
→ CPU has to check the status of the I/O module to know when the device is ready. (handshaking)
→ Wastage of CPU time

② Interrupt-driven I/O :- Processor issues a command to the I/O module, continues to execute other instructions, and is interrupted by I/O module when completed its work.

The CPU suspends the task it was doing, services the request, and returns back to the task it was doing.

Interrupt driven I/O



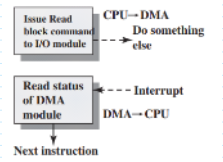
→ Interrupt Service Routine or Interrupt Handler

→ CPU time is not wasted while checking the status.

③ Direct Memory Access :-

I/O module and main memory exchange data directly, without processor involvement.

Direct Memory Access



(c) Direct memory access

Quiz :- In memory-mapped I/O _____

(a) The I/O devices have a separate address space.

(b) The I/O devices and the memory share the same address space.

(c) A part of the memory is specifically set aside for the I/O operation.

(d) The memory and I/O devices have an associated address space.