Lecture - 14 (Mapping Algorithms)

14 February 2024 19:30

Block Placement :-

Where can the block be placed in the cache?

→ determined by mapping algorithm.

Which main memory blocks can reside in which cache memory blocks.

only a small subset of main memory blocks can be held in cache memory.

- Direct Mapping
- Associative Mapping
- (N-way) Set Associative Mapping.

A 2-Level Cache / Main Memory Hierarchy

→ Cache Memory :-

256 blocks/lines of 32 words each

Total size = 8192 (8K) words.

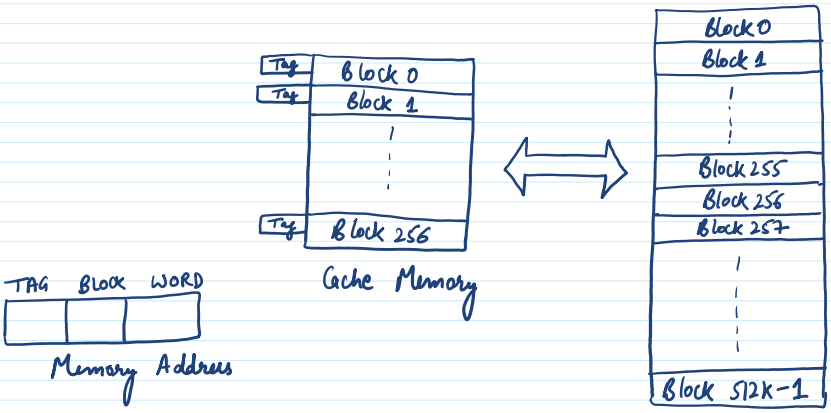
→ Main Memory :-

Total size = 16 M words = 2^{24}

⇒ 24-bit addressable

No. of 32-word blocks = $\frac{16M}{32}$ = 512K

1. Direct Mapping :-



→ Each main memory block can be placed in only one block in the cache.

The mapping function is :—

$$\text{Cache Block} = \frac{\text{(Main Memory Block)}}{\text{(No. of cache blocks)}}$$

→ Direct Memory Address

TAG	BLOCK	WORD
11	8	5

32 Word Memory → 2^5 ⇒ 5 bits for each word

256 Blocks → 2^8 → 8 bits to represent each block.

$$\text{TAG} = \frac{\#\text{ of blocks in Main Memory}}{\#\text{ of blocks in Cache Memory}}$$

TAG → which block of main memory is mapped to a particular block of cache memory.

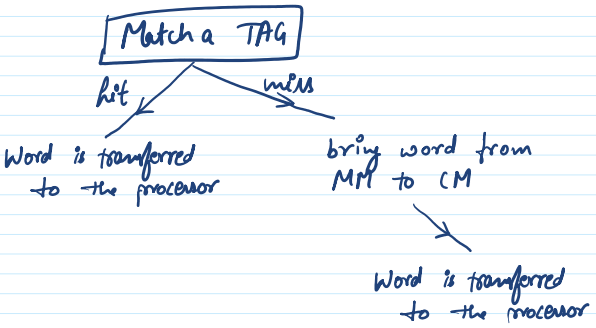
$$\text{TAG} = \frac{512K}{256} = \frac{2^{19}}{2^8} = 2^{11}$$

Mapping $0 \to 0,\ 1 \to 1,\ \ldots,\ 255 \to 255,$

$256 \to 0,\ 257 \to 1,\ \ldots,$

$511 \to 0,\ 512 \to 1,\ \ldots$

Process

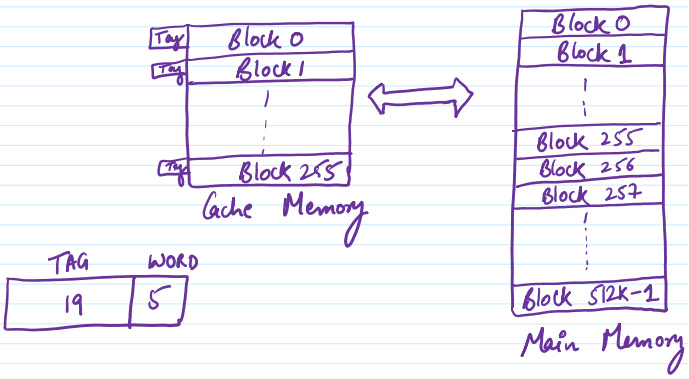


* More than one MM block is mapped onto the same cache block.
→ May lead to contention even if the cache is not full.
→ New block will replace the old block.
→ May lead to poor performance if both the blocks are frequently used.

2. Associative Mapping :-

A MM block can potentially reside in any cache block position.

Memory address



→ When a block is loaded into the MM, 19-bits of the address are stored into the TAG register corresponding to the cache block.

→ When accessing memory, 19-bit TAG of the address

Is compared with all the TAG registers corresponding to all cache blocks.

Advantage :- MM block can reside in any cache block position.

Disadvantage :- Requires associative memory for storing TAG values.
High cost
Lack of scalability

③ N-Way Set Associative Mapping :-

A group of N consecutive blocks in the cache is called a Set.

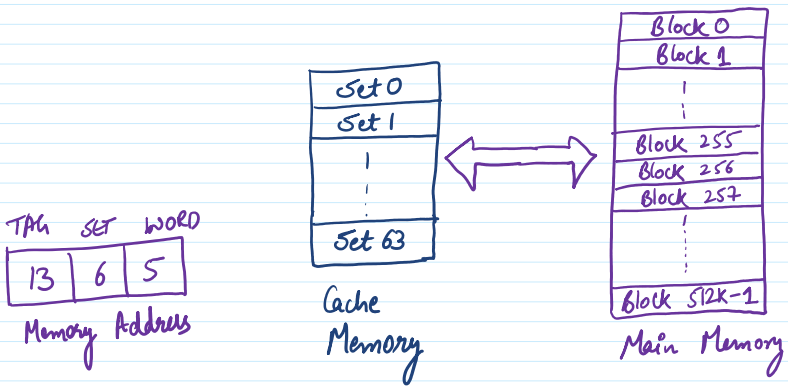
A balance of direct mapping and associative mapping.

A MM block is mapped to a set.

$$\text{Set Number} = \frac{\text{MM Block Number}}{\text{No. of sets in cache}}$$

The block can be placed anywhere within the set.

4-way Set Associative Mapping



$$\text{TAG} = \frac{\#\text{ of Blocks in MM}}{\#\text{ of sets in CM}}$$

$$= \frac{512K}{64} = \frac{2^{19}}{2^6} = 2^{13}$$

4-way Set Associative Mapping :-

# of sets = 64

Set 0 → MM block 0, 64, 128, etc

using %64

can occupy any four available position.

Example -1

4-way set associative

128 Cache Lines

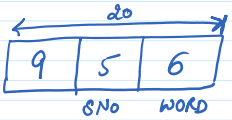
Line size is 64 words

Physical Address is 20-bits

How many bits TAG, SET and WORD field are?

sets = $\frac{128}{4} = 2^5$

Word size = $64 = 2^6$



EXAMPLE 2:-

K-way set associative cache.

Cache contains V sets

The main memory block numbered 'j' must be mapped to any of the cache lines from:-

(a) (j mod k)*v to (j mod k)*v + (v-1)

(b) (j mod v) to (j mod v) + (k-1)

(c) (j mod v) to (j mod v) + (v-1)

(d) (j mod v)*k to (j mod v)*k + (k-1)