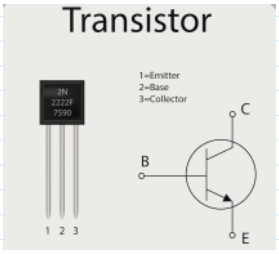
Lecture-11 (Static and Dynamic RAM)

08 February 2024 12:21

Transistors :- Semiconductor device can be used to conduct electric current.



⇒ BJT (Bipolar Junction Transistor)

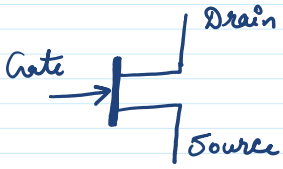
Base :- Used to activate the transistor.

Collector :- Positive Lead

Emitter :- Negative Lead.

⇒ FET (Field Effect Transistor)

Gate, Source and Drain

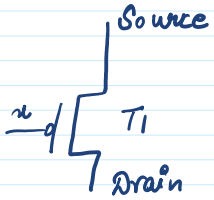


Voltage at Gate controls the current between source and drain.

MOSFET transistors

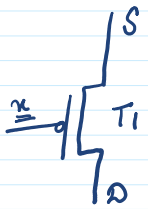
(Metal-oxide-semiconductor field-effect transistor)

PMOS & NMOS Transistors



When x=0

There is conducting path from S to D



When x=1

There is a conducting path from S to D

PMOS v/s NMOS ?

Bistable Latching Circuitry
(flip-flop) to store each bit.

Static RAM :-

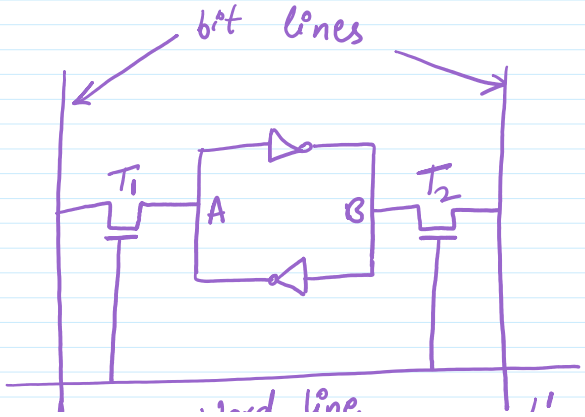
→ Semiconductor memory uses flip-flops to store each bit.

→ Can be arranged in rows and columns of memory cells.
Word line and bit line

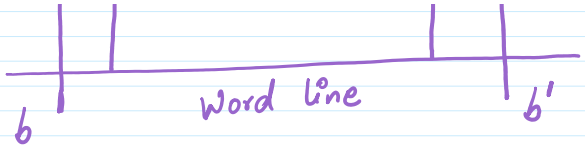
→ Widely used in small-scale systems like microcontrollers

→ Cache Memories

1-bit SRAM Cell



2 pass transistors
4 transistors for inverter pair.

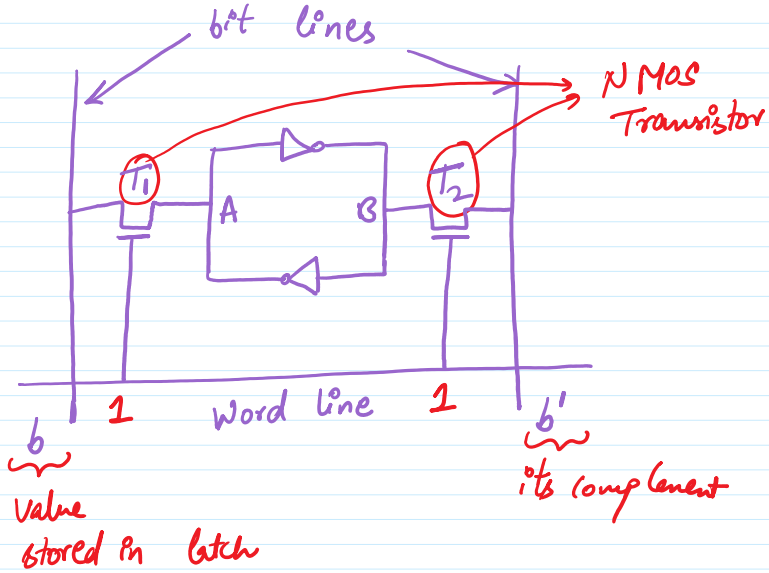


→ Two inverters are cross connected to form a latch

→ Connected to two bit lines with T1 and T2

→ Transistors behave like switches that can be (OFF) and (ON) under the control of word line.

Read operation :—



① To read content of the cell, word line is activated (= 1) ⇒ T1 → ON
T2 → ON

If value is 1 bit-line (b) → 1
bit-line ($\bar{b}$) → 0

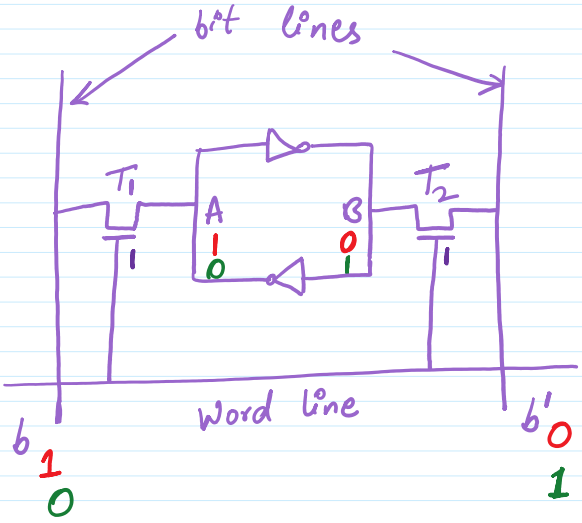
If value is 0 b → 0
$\bar{b}$ → 1

Read / Write signal will monitor the state

of b and $\bar{b}$ to figure out value (0/1)

Write operation :-

Write 1
Write 0

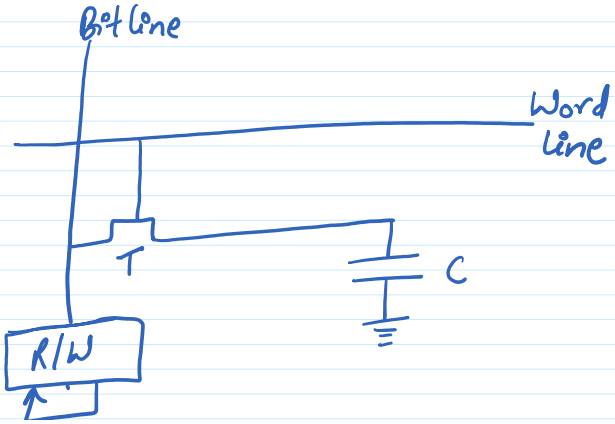


Dynamic RAM :-

→ Do not retain its state even if power supply is ON.

→ Data stored in the form of charge stored on a capacitor.

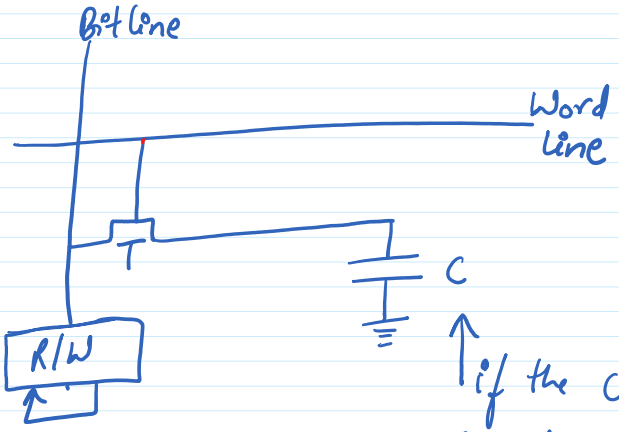
1-transistor DRAM Cell



→ Requires periodic fresh (due to leakage in charge)

→ Less expensive.

⇒ READ Operation in DRAM



→ The transistor of a particular cell is turned on by activating the word line

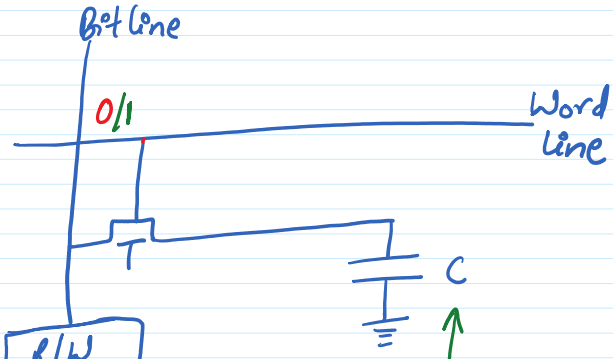
→ R/W control signal will sense the charge stored in the capacitor.

↑ if the charge is above threshold,
⇒ high voltage with logic 1

if below threshold, grounded
logic 0.

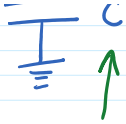
⇒ WRITE Operation in DRAM

To be written:—
0, 1



→ Word line → transistor

→ Depending on the value to be written, (0/1) apply voltage (high/low)



The capacitor gets charged to the required voltage state.

apply voltage (high/low)

⇒ Refreshing of capacitor requires READ-WRITE cycles.

Types of DRAM

- ADRAM (Asynchronous)
  - → Timing of memory is handled asynchronously.
  - A special memory controller.
- SDRAM (Synchronous)
  - → Memory operations are synchronized by a clock.