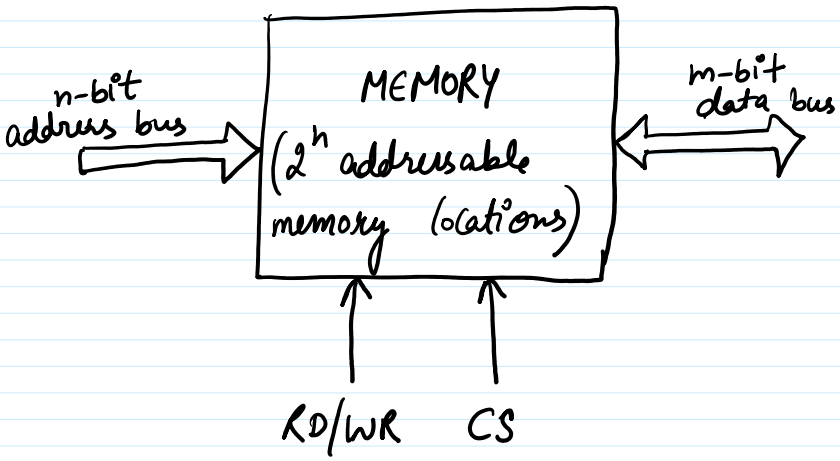
Memory Interfacing :-

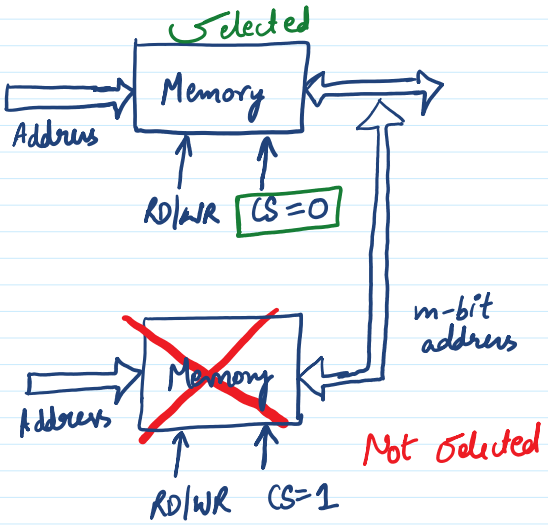
Interfacing more memory modules with the processor.

Questions :-

1. How address and data lines connected to memory module?
2. How address is decoded?
3. Distribution of memory addresses?
4. Speed up of data transfer rate b/w processor and memory.



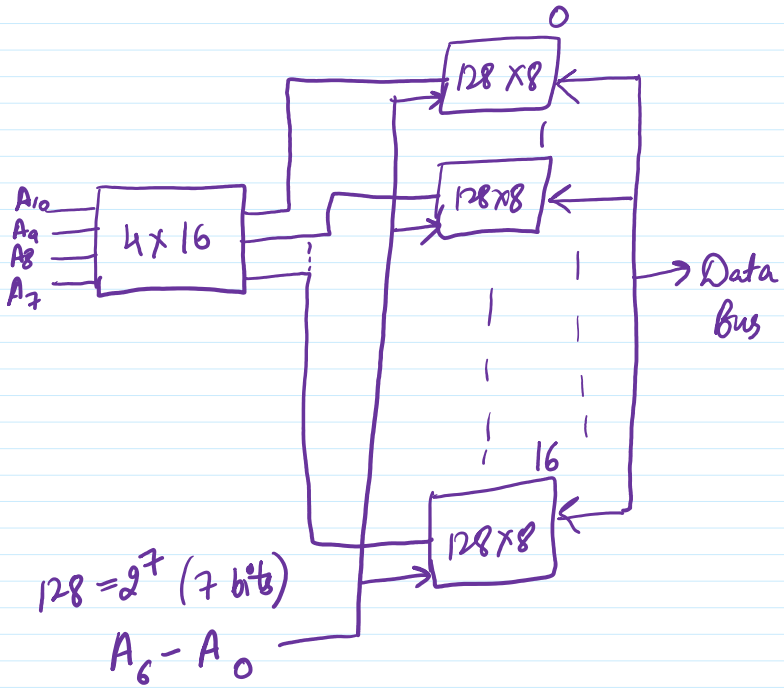
Chip Select (CS) :- Required when there are multiple modules of memory.



⇒ How many 128×8 RAM Chips are needed to provide a memory capacity of 2048×8 ?

$$\frac{2048 \times 8}{128 \times 8} = 16$$

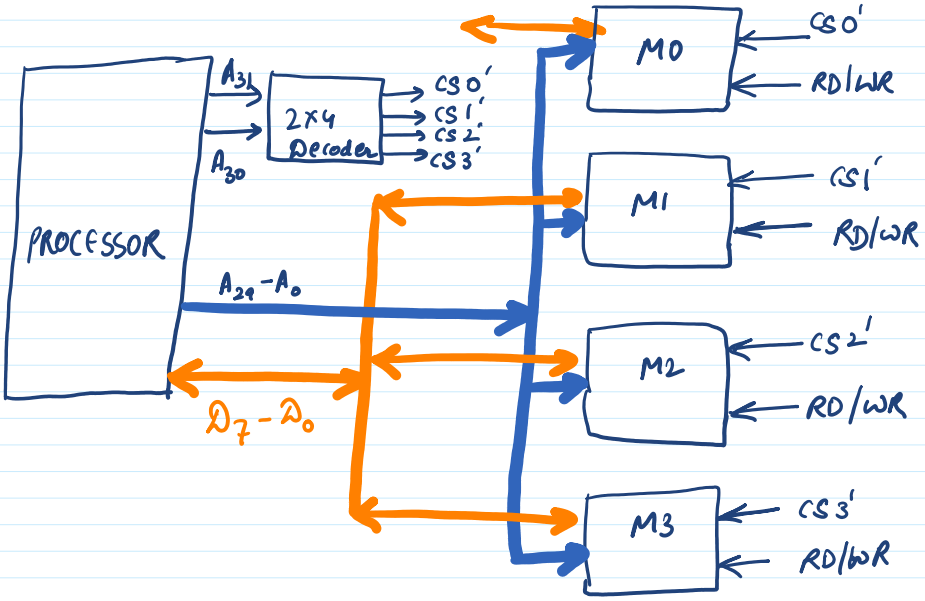
$2048 = 2^{11}$ 11 address bits



⇒ How many 128×8 RAM chips are

required to provide a memory capacity of 2048 x 16 ?

Interface for multiple chips to the processor.



Addresses — 30 bits

M0 → 00 xxxxxxxxxx ... x

M1 → 01 xxxxxxxxxx ... x

M2 → 10 xxxxxxxxxx ... x

M3 → 11 xxxxxxxxxx ... x

What is the range of addresses for M0, M1, M2, M3 ?

Memory latency and bandwidth :-

① Let latency $L = 20$ ns per 32-bit word.

Bandwidth (BW)?

Max bytes can be transferred per unit time.

$$BW = \frac{32}{20 \times 10^{-9}} = \_\_\_ \text{ Mbytes/sec}$$